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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/619,988	07/15/2003	Giora Biran	IL920000077US1	8803

7590 10/12/2005

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EXAMINER	
CHEN, ALAN S	
ART UNIT	**PAPER NUMBER**
2182	

DATE MAILED: 10/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/619,988	BIRAN ET AL.	
	Examiner	Art Unit	
	Alan S. Chen	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 08/04/2005 have been fully considered but they are not persuasive.

2. Applicant mainly argues (i.e., on pg. 8 as well as pg. 10 of Remarks) that Garcia is only storing descriptors and not generating descriptors as specified by the claims.

Examiner does not agree. Garcia clearly provides mechanisms to generate/create plurality of the descriptors. Garcia discloses creating a linked list, e.g., a plurality of descriptors. Column 12, lines 62+ disclose creating/generating values in the descriptors in order to make up the link list. The chain pointer, Fig. 5, element 54, serves as a reference for locating and retrieving the next CDB as indicated in Column 13, lines 1-3. Column 14, lines 23+ disclose the multi-channel adapter unit generating the chain pointer in part to assist in establishing the linked list. Prior to these actions by Garcia, the descriptors were merely a random disparate collection of descriptors no necessarily associated with each other. In applicant's claims regarding the generation of descriptors, particularly claim 1, they recite simply "...descriptor logic for generating a plurality of descriptors including a frame descriptor defining a data packet to be communicated between a location in the memory and a second data processing system". Garcia covers this broad language. The descriptor logic is intrinsically present, represented by the hardware that performs the creation of values that go into each descriptor to form/generate the entire linked list, e.g., flow chart and hardware configurations shown in Figs. 6-11. The plurality of descriptors is indeed generated when the linked list is created which assembles and associate multiple descriptors together, by definition "generating a plurality of descriptors". Fig. 5,

elements 52-54 shows the "frame descriptor", since the elements 52-54 literally represent a frame where the information located within represent where the data block shown in Fig. 5, e.g., the data packet, should go. Column 11, lines 1-25 disclose the MAU, being a separate data processing system as Figure 1 shows the MAU clearly separated from other systems only to communicate with them over a bus, where the MAU processing the CDB which has the data pointer, element 52 that points the CDB to a location in the memory, element 3, indicated as the block storage space CDSB in Fig. 1. This is enough to meet "...frame descriptor defining a data packet to be communicated between a location in the memory and a second data processing system". The "pointer descriptor" as stated in the rejection can be identified as the data pointer in Fig. 5, element 52 since it points to the address/location in memory, Fig. 1, element 8. Lastly, the descriptor table is the CDT shown in Fig. 3, element 30, that is in the MAU, the second data processing system, that will be accessed by the memory and first processor, e.g., the first data processing system. The applicant argues the CDT as explicitly stated by Garcia is not a "descriptor table" but merely a table (pg. 10, last paragraph). Examiner points out that CDT stands for "channel descriptor table" and that the claim language only requires at least one of the descriptors to be in the CDT, not requiring everyone of the generated descriptors to be stored, even physically stored, in the table. Indeed, the head and tail pointers represent the linked list of CDBs in the CDT of Fig. 4 and thus meet the terminology of storing the descriptors in the table. Note also that the MAU puts the next CBD in the CDT based on what is the current CDB that is being processed (Fig. 7, element 73).

Nowhere in the claims disclose the details of what applicant construes as "generating a plurality of descriptors", e.g., the applicant is apparently arguing the descriptors in their entirety

are generated from scratch. However, under the broadest reasonable interpretation of the claims, this is not what the claim language state. The claims are sparse in defining what exactly "generating" descriptors entail. Garcia provides the act of adding/modifying the command descriptors and tables, and the fact that it assembles the plurality of descriptors into a linked list, all are enough to read on the applicants broad limitations regarding the generation of descriptors.

Regarding the control of the flow of data between the memory of the host computer system and the data communication interface, which the Examiner construes to be the MAU, the CDBs are transferred to the MAU as shown in Fig. 13, the CDB being fetched from memory. The fetches from the CDBs are based on the order of the linked list, and this is first initiated by the CDT having a pointer to the first CDB.

The applicant's remaining arguments are along the same vein as what is answered above and also allege the use of hindsight. It is evident Garcia is anticipatory, showing all the elements of what is claimed in the instant application thus hindsight is not used. The Examiner reiterates his rejection in detail below.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-20 rejected under 35 U.S.C. 102(b) as being anticipated by No. 5,448,702 Garcia.

5. As per claims 1 and 10, Garcia discloses an apparatus and method (Fig. 9) comprising: descriptor logic (Fig. 2-4 shown how descriptors are implemented, e.g., in form a linked list and pointer; Fig. 5 shows the components of a descriptor), said apparatus for controlling flow of data between first and second data processing systems via a memory (Column 18, lines 53-65, the adaptor in Fig. 9 is connected to the processor and memory which it assists in communications with DMA, the processor is in Fig. 1, element 2 and memory is Fig. 1, element 3, either the processor or the MAU adaptor device can be construed to the first or second device), said descriptor logic for generating a plurality of descriptors including a frame descriptor defining a data packet to be communicated (Frame descriptor is shown in Fig. 5, element 52-55, where it dictates where to point the data to next and the amount of data in the packet) between a location in the memory and the second data processing system (Column 4, line 62-Column 5, line 10, where the apparatus in Fig. 5 transfers descriptors in memory to a plurality of peripheral devices, e.g., other data processing systems), and a pointer descriptor identifying the location in the memory (Fig. 5, element 52 or 54); and a descriptor table (Fig. 4) for storing the descriptors generated by the descriptor logic for access by the first and second data processing systems (contains a linked list of descriptors).

6. As per claims 2,3,11 and 12, Garcia discloses claims 1 and 10, wherein the descriptor table is stored in the data processing system (Fig. 3, stored in adaptor registers, Fig. 9 is the MAU).

7. As per claims 4-6, 13 and 14, Garcia discloses claims 1 and 10, wherein the descriptor logic generates various branch descriptor comprising links to other descriptors in the descriptor table (Fig. 3, various descriptors shown branching/pointing to the next descriptor).

8. As per claims 7 and 15, Garcia discloses claims 1 and 10, wherein the first data processing system comprises a host system (Fig. 1, processor 2 and memory 3 is the host processing system).

9. As per claims 8 and 16, Garcia discloses claims 1 and 10, wherein the second data processing system comprises a data communications interface for communicating data between the host computer system and a data communication network (Column 9, lines 1-8, adaptors are attached external networks).

10. As per claim 9, Garcia discloses a data processing system (Fig. 1) comprising a host processing system having a memory (element 3), a data communications interface (Fig. 1, element 4.5) for communicating data between the host computer system and a data communication network (Column 9, lines 1-8), and apparatus according to claim 1.

11. As per claims 17-20, Garcia discloses a computer program product, article of manufacture and program storage device readable by a machine (Fig. 1, shows computer product the result of manufacture, where the processor inherently requires initial instruction, e.g., booting and initialization, in order to start operation) in accordance to claims 1, 9 and 10.

Conclusion

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alan S. Chen whose telephone number is 571-272-4143. The examiner can normally be reached on M-F 8:30am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim N. Huynh can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ASC
10/06/2005

KIM HUYNH
PRIMARY EXAMINER